

Technical Manual

DAP-010/020/040/090

ALPHANUMERIC POCSAG PAGER

Contains Operating and Technical information

DURETECH CO., LTD

DAP- 0x0
Instruction Manual

DURETECH CO.LTD

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1

General Information

Introduction

This section contains general information about the DAP-0X0 manufactured by duretech co.,ltd.

The DURETECH DAP-0X0 is character and numeric display pager receiver who employs paging system that complies with the POCSAG PROTOCOL system.

The DAP-0X0 uses single AAA battery and operates in the VHF, UHF band frequency range.

DAP-010 A band : 139Mhz Band
B band: 147Mhz Band
C band : 155Mhz Band
D band: 163Mhz Band
E band: 171Mhz Band

DAP-020 : 281Mhz Band

DAP-040 : 400Mhz Band

DAP-090 : 930Mhz Band

DAP-0X0 is PLL(Phase Locked Loop) local oscillator method use.

The rest of section 1 is arranged in the following manner:

- Features
- Manual addenda
- Specifications

Features

The following features are in the DURETECH DAP-0X0 character display pager.

- POCSAG alphanumeric multi-lingual pager
- Simultaneous display alphanumeric(ASCII) and Numeric.
- Dot matrix LCD graphic character.
 - 2 row X 12 Characters (in Thailand)
 - 2 row X 15 Characters (with English)
 - 2 row X 12 Characters and 4 row X Characters are selectable in Russia.
- 8 kind of alert and melody.
- Memory capacity: More than 25,000 Characters in ASCII
- User selectable Alert / Vibration / Sleep mode.
- LCD Illumination (Lamp back light)
- Low battery alerts display
- Out of service area indication.
- Year, month, date and day of the week display.
- Alarm function (Melody & Alert tone)
- Mail receiving On/Off.
- Message management.
 - Page Up/Down
 - Memory full indication
 - Message deletes (Whole or individual)
 - Duplicate message indication
- User selectable LCD bright.
- Decode IC added to CPU.

Manual addenda

Any improvements or changes concerning the card or manual will be explained in an addendum included with the card. Addenda are provided in a page replacement format. Replace the obsolete pages with the new pages.

Specifications

DAP-0X0 specifications are found at the technical parts of this manual. These specifications are exclusive of the mainframe specifications.

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Operation

Introduction

This section covers the basic operation for DAP-0X0 with DURETECH alphanumeric pager.

The information in this section is formatted as follow:

- Basic Description
- Appearance Description
- Source power
- Controls and Indications
- Operations

Basic Description

The DAP-0X0 character display pager is designed with compact size as well as user friendly graphic icon functions. So excellent readability and easily operational key functions will provide better approach to user.

The capcode is reprogrammed by DAP-0X0 program package through software support of IBM compatible personal computer,;

Appearance Description



Source Power

The DAP-0X0 uses single AAA battery.

Controls and Indications

Escape Button

- Escape to before mode or previous message.
- Back light tune on after continuous push.

Read Button

- Reading if receiving message
- Setting of minute, hour, am/pm for time or alarm
- Message page down
- Power off

Left / Right Button

- Selection of function on LCD icon.
- Selection of each item at function state.

Operations

Refer to user's manual of DURETECH DAP-0X0 alphanumeric display pager.

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Technical Parts

Introduction

This section contains information necessary to technical the DURETECH DAP-1X0 and is arranged as follows:

- General Description
- Electrical Specification
- Pocsag Protocol Description
- Block diagram Description
- Circuit Description

General Description

The DAP-0X0 pager is double-super heterodyne FM receiver which uses digital signal system for message.

The power is supplied by a single AAA size 1.5V battery.

Electrical Specification.

DAP-010

Frequency range: 135- 174 MHZ

Channel space: 25KHZ

Modulation: FM 4.5KHZ

Intermodulation: more then 55dB

Capcode capacity: 6 capcode

Paging sensitivity: 5uV/m at 512 BPS

7uV/m at 1200 BPS

9uV/m at 2400 BPS

Spurious Rejection: more then 60dB

Image rejection: more then 50dB

Selectivity: more then 60dB

Frequency stability: +-5PPM(-10degree to +50 degree)

Alert tone level: more then 80dB at 30 cm distance

Code format: POCSAG

Baud rate: 512, 1200, 2400BPS each single mode

Power supply: Single AAA size

Battery life: more then 25Days

Dimension: 60(w) X 40(H) X 18.3(T)

Weight: 46g (Including battery and holster)

DAP-020

Frequency range: 279 - 281 MHZ
Channel space: 25KHZ
Modulation: FM 4.5KHZ
Intermodulation: more then 55dB
Capcode capacity: 6 capcode
Paging sensitivity: 5uV/m at 512 BPS
7uV/m at 1200 BPS
9uV/m at 2400 BPS
Spurious Rejection: more then 60dB
Image rejection: more then 50dB
Selectivity: more then 60dB
Frequency stability: +-5PPM(-10degree to +50 degree)
Alert tone level: more then 80dB at 30 cm distance
Code format: POCSAG
Baud rate: 512, 1200, 2400BPS each single mode
Power supply: Single AAA size
Battery life: more then 25Days
Dimension: 60(w) X 40(H) X 18.3(T)
Weight: 46g (Including battery and holster)

DAP-040

Frequency range: 402 - 512MHZ
Channel space: 25KHZ
Modulation: FM 4.5KHZ
Intermodulation: more then 55dB
Capcode capacity: 6 capcode
Paging sensitivity: 5uV/m at 512 BPS
7uV/m at 1200 BPS
9uV/m at 2400 BPS
Spurious Rejection: more then 60dB
Image rejection: more then 45dB
Selectivity: more then 60dB
Frequency stability: +-5PPM(-10degree to +50 degree)
Alert tone level: more then 80dB at 30 cm distance
Code format: POCSAG
Baud rate: 512, 1200, 2400BPS each single mode

Power supply: Single AAA size
Battery life: more then 25Days
Dimension: 60(w) X 40(H) X 18.3(T)
Weight: 46g (Including battery and holster)

DAP-090

Frequency range: 929 - 932 MHZ
Channel space: 25KHZ
Modulation: FM 4.5KHZ
Intermodulation: more then 50dB
Capcode capacity: 6 capcode
Paging sensitivity: 5uV/m at 512 BPS
7uV/m at 1200 BPS
9uV/m at 2400 BPS
Spurious Rejection: more then 50dB
Image rejection:: more then 40dB
Selectivity: more then 50dB
Frequency stability: +-5PPM(-10degree to +50 degree)
Alert tone level: more then 80dB at 30 cm distance
Code format: POCSAG
Baud rate: 512, 1200, 2400BPS each single mode
Power supply: Single AAA size
Battery life: more then 25Days
Dimension: 60(w) X 40(H) X 18.3(T)
Weight: 46g (Including battery and holster)

CAUTION

For good performance, this option is changeable notice.

Pocsag protocol description

Pocsag code

POCSAG is constituted to suggest the standard code and to decide the international radio paging signal format.

The standard paging code is POCSAG CODE which is being regulated in CCIR Recommendation 584.

*POCSAG mean to post office code standardization advisory group.

POCSAG digital paging signaling format

Transmission will be consist of preamble and sequencing batch (synchronization code word + 8 frame =17 code words) Each batch will be started with synchronization code (SC). Transmission format for signal is shown on figure. And if there is no further call, signal transmission will be stopped.

Preamble

Each transmission starts with a preamble to aid the pagers to attain bit synchronization and thus help in acquiring word and batch synchronization. The preamble is a pattern of reversals, 1010101010... repeated for a period of at least 576bits, the duration of a batch plus a code word.

Batch structure

Code words are structured in batches, which comprise a synchronization code word followed by 8 frames, each containing 2 code words. The frames are numbered 0 to 7 and pager population is divided into 8 groups. Thus each pager is allocated to one of the 8 frames according to the 3 least significant bits (LSB) of its 21 bit identify.

Type of code words

Code words contain 32 bits, which are transmitted with the most significant bit first.

Refer to figure

Synchronization

The following table shows the synchronization code word

Address code word

The structure of address code word is shown on figure Bit1 of an address code is always zeroing. This distinguishes it from a message code word. Bit2-19 is address bits corresponding to the 18 most significant bits of a 21 bit identify assigned to the pager.

Bit 3 LSB will not be transmitted, but it will be used to decide the frame of address code word, which will be transmitted.

The total number of code identify is about 2,000,000. Bit 20 and 21 are the two function bit which are used to select the required address from the four assigned to the pager, the total number of address is 2. Bit 22 to 31 are the parity check bit and the Bit32 is chosen to give even parity.

Message code word

The structure of message code word is shown in figure 2-2. A message code word always starts with a one and the whole message always follows directly after the address code word. The framing rules of the code format do not apply to a message code words continue until terminated by the transmission of the nest address code word or idle code word. Each message code displaces at least one address code word and idle code word and the displaces address code words are delayed and

transmitted in the next available appropriate frame.

Although message code words may continue into the next batch, the normal batch structure is maintained. The batch will consist of 16 code words, preceded by a synchronization code word. At the conclusion of a message any waiting address code words are transmitted, starting with first appropriate to the first free frame or half frame. Message code words have 20 message bit, via bit 2 to bit 21 inclusive and there are followed by the parity check bit and even check bit.

Idle code word

In the absence of an address code word or message code word, an idle code word is transmitted. The idle code word is a valid address code word, which must not be allocation to pagers and following structure.

Code word generation

Each code word has 21 information bits, which correspond to the coefficients of a polynomial having terms from X^{31} down X^{10} . This polynomial is divided Modulo-2, by the generation polynomial $X^{10} + X^9 + X^8 + X^8 + X^6 + X^5 + 1$. The check bits correspond to the coefficients of the terms from X^9 to X^0 in the remainder polynomial found at the completion of this division.

The complete block, consisting of the information bits followed by the check bits, corresponds to the coefficients of a polynomial, which is integrally divisible in modulo-2 fashion by the generating polynomial. One additional bit is added to the 31 bits of the block to provide an even bit parity check for the whole code word.

BCH error correcting and detection

Detect and correct and detection

Numeric message format

The numeric format is provided for the transmission of message, which may be represented solely in decimal numerals together with space, hyphens, opening, closing brackets, urgency symbol and an other symbol. The bits of each character are transmitted in the same order as they are to be read are packed 5 per message code word. Any unwanted part of the last code word of the message is filled with space characters.

Technical Description

Introduction

This section contains RF and Digital board about hardware for DAP-0X0 with DURETECH pager.

General Description

The DAP-0X0 is structure double super heterodyne FM receiver with uses digital signal system for message. The power is supplied by a single AAA size 1.5V battery. Decode added to MCU. And local oscillator is PLL.

RF parts

FM Deviation: 4.5KHZ

1st IF: 21.4MHZ

2nd IF: 455KHZ

1st local oscillator frequency: $F_{lo} = (F_c - 21.4\text{MHZ})$

VCO frequency: $F_{vco} = (F_c - 21.4\text{MHZ}) / X$

X mean to 2: 100M Band

4: 200M Band

6: 400M Band

12: 900M Band

2nd local oscillator frequency: 20.945MHZ

Do not automatically antenna tuning.

VCO variable tuning voltage: 1.5V.

Logic parts

Input voltage: 1.3V – 1.5V

Logic driving voltage (D/D convert output voltage): 2.7V.

TABLE 1-1

MODEL	SAW	Freq range
DAP-010	KSF139AC1	139MHZ ± 4MHZ
DAP-010	KSF147AC1	147MHZ ± 4MHZ
DAP-010	KSF155AC1	155MHZ ± 4MHZ
DAP-010	KSF163BC1	163MHZ ± 4MHZ
DAP-010	KSF171AC1	171MHZ ± 4MHZ

Circuit Description

RF Board

Antenna (ANT111)

The antenna is a single loop design, which encircles the bottom of the main frame at the circuit board assembly.

This antenna is designed to the peak at the desired signal and connected to the RF amplifier. Tuning frequency is determined by the antenna tuning variable capacitor (VC111).

RF amp (Q111, 112)

The signal received by the loop antenna is input to the amplifier circuit which formed by two transistors (Q111, 112). This amplifier is a low noise and high gain amplifier. Gain is about 12dB.

Band Pass Filter1 (F111)

The extraneous signals such as image and spurious are amplified by the RF amp and attenuated by approximately 60dB by SAW filter, which is low insertion loss characteristics. In addition, extraneous radiation from the unit is suppressed by the SAW filter.

*SAW filter means surface acoustic wave.

*Refer to table 1-1, 1-2 of SAW range

TABLE 1-2

MODEL	SAW	Freq range
DAP-040	KSF450AC1	450MHZ ± 2MHZ
DAP-040	KSF466AC1	466MHZ ± 2MHZ
DAP-040	KSF448AC1	448MHZ ± 2MHZ
DAP-040	KSF458BC1	458MHZ ± 4MHZ
DAP-040	KSF410AC1	410MHZ ± 2MHZ
DAP-040	KSF446AC1	446MHZ ± 2MHZ
DAP-040	KSF454BC1	454MHZ ± 4MHZ
DAP-040	KSF474AC1	474MHZ ± 2MHZ

PLL Description

In the local oscillator circuit is 3rd overtone PLL oscillator which is a VCO circuit and the target frequency is filtered by the LPF via SM5166AV. Figure 3-1 is PLL sequence diagram. And PLL sub-description as shown in figure 3-1.

Local oscillator

Local oscillator makes frequency wave as F_{lo} for 1ST mix. And local oscillator frequency is carrier frequency minus 21.4MHZ.

$$F_{lo} = (F_c - 21.4\text{MHZ})$$

F_{lo} means to local oscillator frequency.

F_c means to carrier frequency

21.4MHZ are 2nd IF.

VCO

VCO is voltage control oscillator. VCO voltage adjusts VC112 using ceramic screwdriver. VCO oscillator frequency is as follow:

$$\text{VCO frequency: } F_{vco} = (F_c - 21.4\text{MHZ}) / X$$

X mean to 2: 100M Band

4: 200M Band

6: 400M Band

12: 900M Band

LPF (LOW PASS FILTER)

An external low pass filter connects to DOP. The output from the filter is fed to a voltage-controlled oscillator (VCO) which generates the PLL output.

Input data

The control data input uses a 3line 17bits serial interface comprising the clock (CLK), data input (DATA) and latch enable (LE).

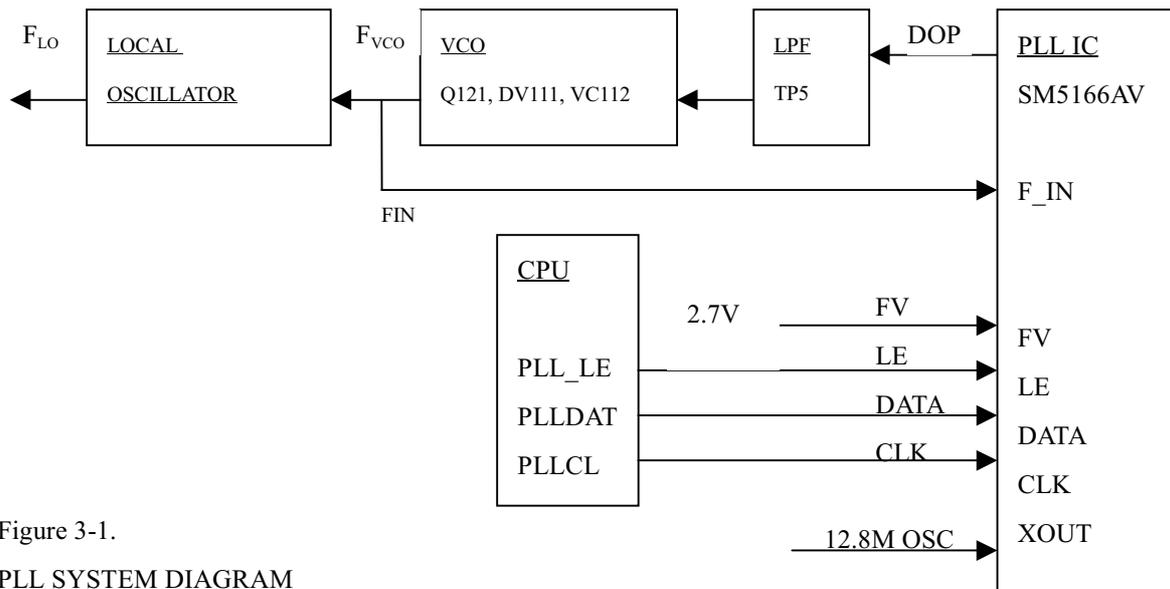


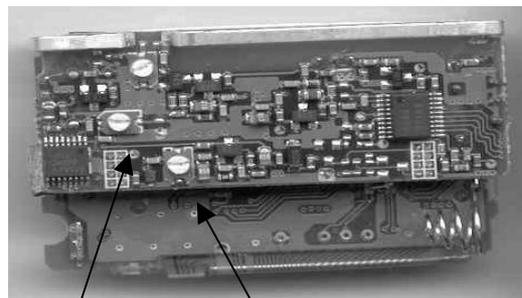
Figure 3-1.
PLL SYSTEM DIAGRAM

PLL IC Description

IC model: SM5166AV

Pin description:

Number	Name	Description
1	XIN	Reference frequency divider 12.8MHZ x-tal connector pin.
2	XOUT	The clock is output on XOUT
3	VDD3	Phase detector, charge pump and boost-up signal 2.7V supply.
5	DOP	Phase detector output pin.
6	VSS	Ground
7	FIN	Operating frequency divider input pin
8	VDD1	Prescaler and counter 1V supply.
11	CLK	Control data clock input pin
12	DATA	Control data input pin
13	LE	Control data latch enable signal input pin
14	FV	Power saver control pin.



TP5

VC112

Mixer

Mixer circuit is that F_c convert to IF.

$$IF = F_c - F_{LO} = 21.4\text{MHZ (1'ST IF)}$$

IF IC (KA8514D)

VCO Tuning Methods

Positioned board on the test fixture and connect test equipment as follow.

Set the S.S.G frequency to F_c and deviation to FM 4.5KHZ.

Set audio frequency to preamble on, then set the RF amplitude level -60dBm.

Set oscilloscope probe to TP5 on the RF PCB.

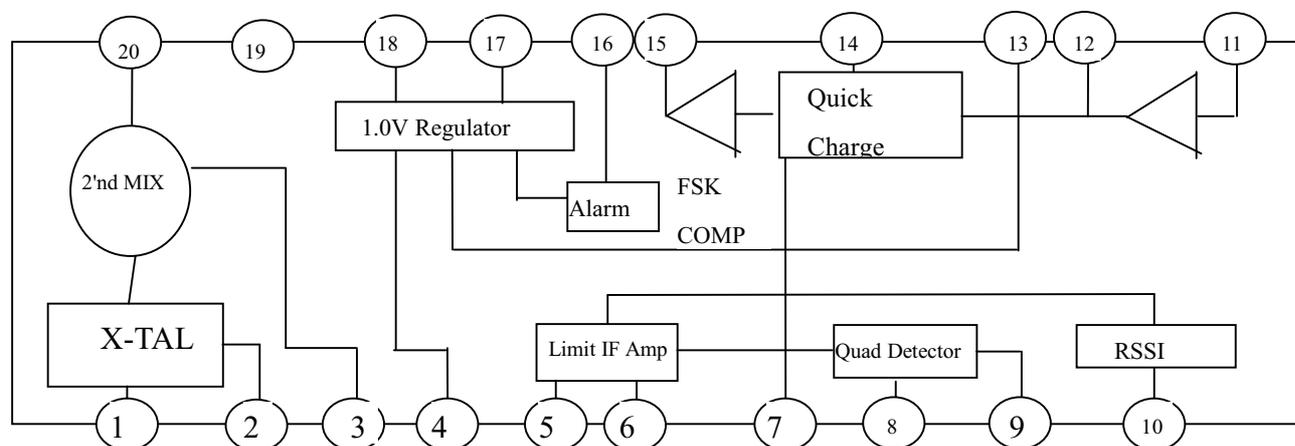
Tune the VCO voltage to 1.5V by VC112.

Introduction

The KA8514D is designed for FM IF detection on the pager set. It includes voltage regulator, low battery detection circuit, Mixer, Oscillator FSK comparator and limiting IF amplifier.

Block diagram

Refer to Figure 3-3.



Pin Description

pin no	symbol	description
1	osci	Oscillator input
2	osco	Oscillator output
3	mo	Mixer output pin
4	Vcc	Vcc pin
5	Li	IF limiter amplifier input
6	LD	Bypass capacitor connect pin for the IF limiter amplifier
7	FSKI	Differential Amp Reference input on the FSK comparator
8	QD	Quadrature detection phase shifter pin.
9	RAO	Recovered audio signal output.
10	RSSI	Output pin for RSSI.
11	LFPI	Low pass filter amplifier input.
12	LPFO	Low pass filter amplifier output
13	BSC	Battery saving control pin.
14	QC	Quick charge control pin.
15	FSKO	FSK signal output pin.
16	AO	Alarm output.
17	REGC	External transistor control pin.
18	REGO	Regulated voltage output
19	GND	Ground.
20	MI	mixer input.

IF Detector Description

The KA8514 consists of 2nd mixer, a discriminator, a low pass filter, data comparator, a battery saving circuit, low battery detection, voltage regulator and RSSI function. AF signal extracted from the discriminator part, goes to the low pass filter. The FSK signal extracted by the comparator, goes to decoder.

Quadrature Detector

The detector is a quadrature type. The 455khz discriminator circuit must be provided externally.

2nd local Oscillator

2nd local oscillator is operating by the 20.945MHZ crystal oscillator connected between pin1 and pin2 with IF IC (KA8514).

FSK out

FSK demodulation can be accomplished by the internal comparator. The output of the comparator will be the logical output. The comparator is a non- inverting type with an open collect output.

Low pass filter

Low pass filter passed cutoff frequency of audio signal. Cutoff frequency is 256Hz as 512bps, 600Hz as 1200bps and 1.2KHz as 2400bps. And about each BPS, changed value as follow.

BPS	R112	R123	R124	C134	C135	C136
512	100K	100K	100K	1000P	0.022uF	5600P
1200	68K	68K	68K	560P	0.01uF	3300P
2400	47K	47K	47K	470P	6800P	2700P

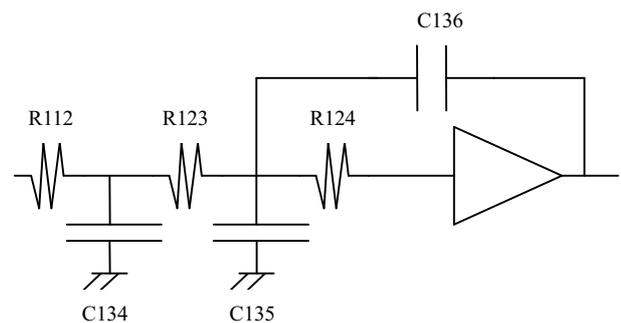


Figure 3-5 LPF

Local and Antenna Tuning method

Positioned board on the test fixture and connect test equipment as follow.

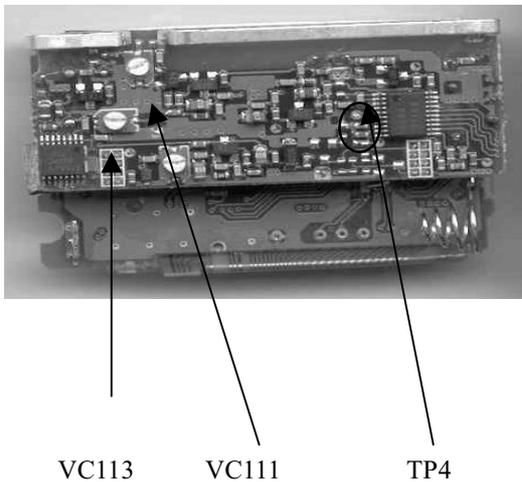
Set the S.S.G frequency to F_c and deviation to FM 4.5KHZ.

Set preamble on, then set the RF level -50dBm .

Tune the local tuning variable capacitor (VC113) to frequency 455khz at frequency counter

Tune the antenna tuning capacitor (VC111) to max level 455KHZ sine wave form.

Repeat adjustment several times for wanted sensitivity.



Troubleshooting

Cannot receiver

1. Check the 12.8Mhz x-tal (X111)

Check method

Set probe X10 and pick the x-tal lead.

If do not wave form then it is defect. So, change the X-tal.

2. Check the vco voltage.

Normally, VCO voltage is about 1.5V.

If Cannot voltage display, check the trimmer (VC113)

2. Wrong band frequency.

Check the frequency and SAW filter.

3. CN112 8pin connector cool-solder.

Low sensitivity

1. Tune the antenna tuning.

2. Tune the local oscillator (455KHZ)

3. Wrong baud speed.

No sound

1. Check the connector (CN112)

2. Check the buzzer.

-Buzzer cool-solder

No vibration

1. Check the connector (CN112)

2. Check the motor.

Digital board

Block Diagram

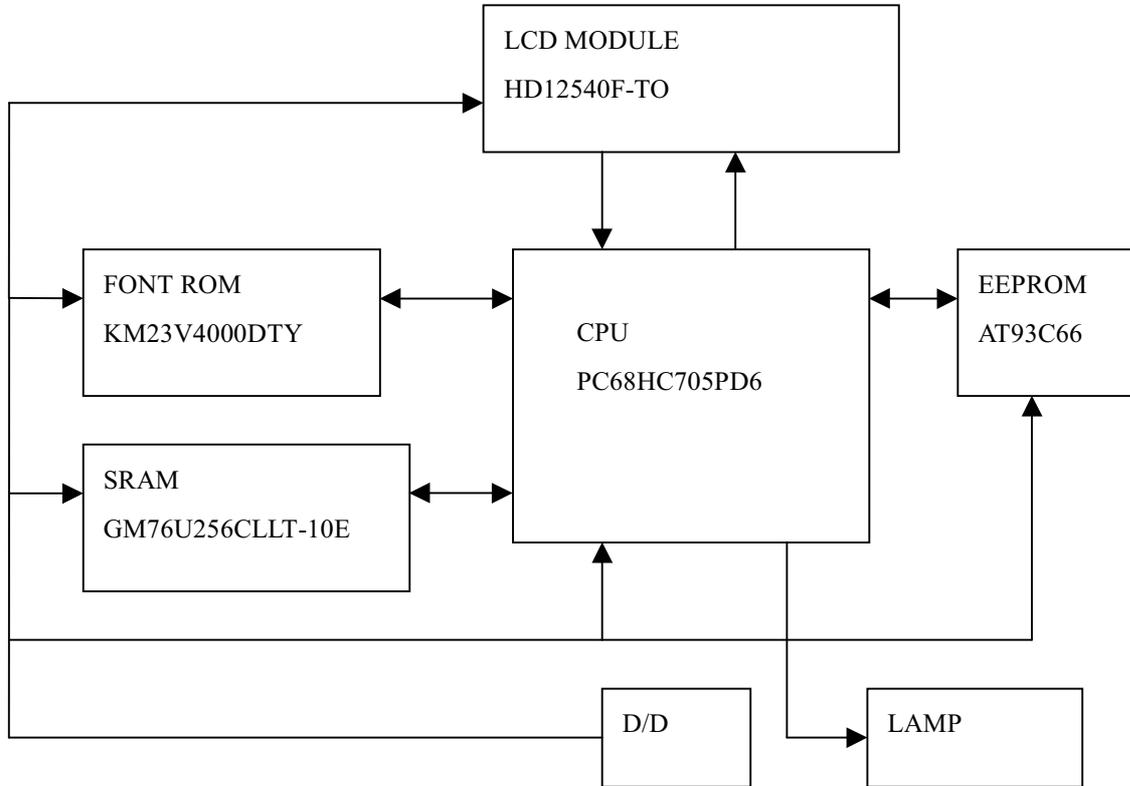


Figure 3-7 DIGITAL BOARD BLOCK DIAGRAM

Circuit Description

DC/DC converter

D/D converter rises voltage from 1.5V to 2.7V.



CPU

The CPU is main process with pager and it contains a POCSAG decode. The CPU main clock provided 2Mhz and 76.8Khz. X201 is oscillated from 76.8khz for data processing and time control in LOW clock frequency.

X202 is oscillated from 2Mhz for MCU operation in high clock frequency.

EEPROM

EEPROM storage capcode, frequency data etc.

SRAM

SRAM storage data with received signal.

FONT ROM

FONT ROM contains each country characters.

Country are English, Thai, china, Russia, Spanish, Portugal.

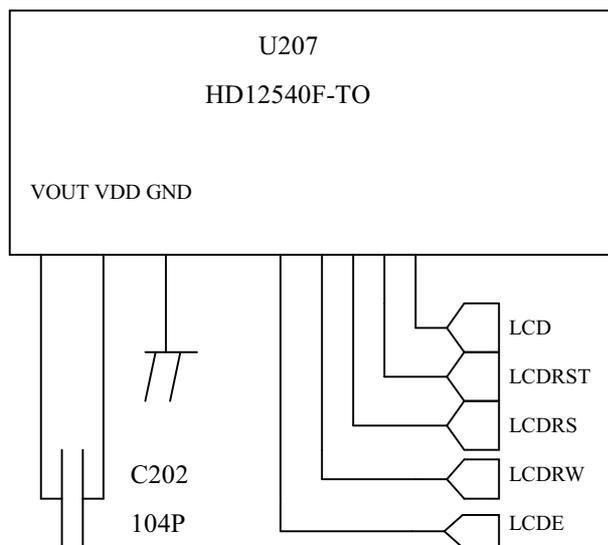
TROUBLE SHOOTING

1. LCD Display is defected

(1) Check lamp

If lamp is on, problem is LCD MODULE and around circuit, another circuit is no problem.

(2) Check LCD MODULE input voltage.



Normal input or output voltage is as follow.

LCD CS: 2.7V

LCD RST: 2.7V

LCDRS: 2.7V

LCDRW: 2.7V

LCDE: 2.7V

VDD: 2.7V

VOUT: 7V

If VOUT voltage is not 7v, short or LCD

MODULE defect. So, changed the LCD module.

Another voltage is not input, then checked the CPU (U203), sometimes CPU lead short.

2. KEY DEFECT(The button is out of function)

(1) Check the key1, key2, and key3 voltage.

Voltage is 2.7V

(2) Push to button, if each button is out of function that your try as follow.

1) KEY1,2,3 and ESC button is defect.

Check to 2M-resonator (X202)

Check method

Set oscilloscope probe set 10X and pick the 2M resonator (X202) land then look at the wave form on scope.

If not oscillated waveform, change the 2M RESONATOR (PBRC-2.00BR)

2) KEY1, 2 and 3 button is defect.

27pin(GND) is cool-solder.

3) Each key is defect.

Each key is cool-solder.

(3) Button fail

Wrong assembly to buttons.

LCD MODUL PIN 27, 28, 29 and 30 cool solders

3. Cannot program

Check the CPU pin 39, 40 and program fixture.

4. Lamp defect

Check the lamp (LP201, 202)

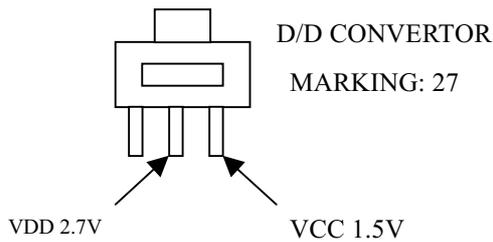
5. No power (Not operating)

1) Check the D/D converter.

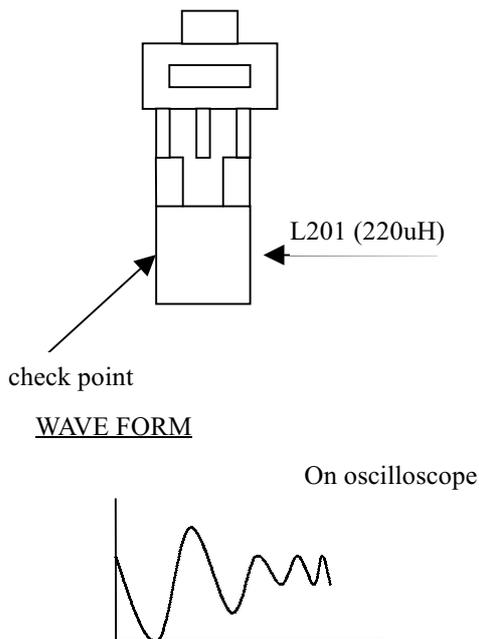
Check Method

Set the oscilloscope or voltage meter for voltage check.

Check 2.7v as pin2 and 1.5v as pin 3 with D/D converter. (U205)

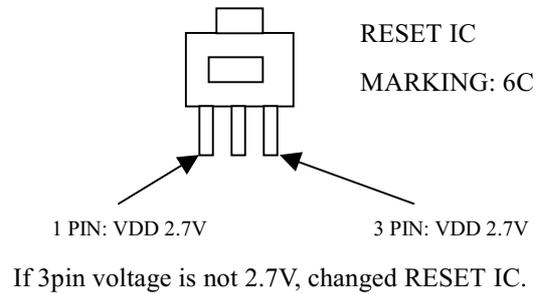


Check the L201 (220uH) and waveform.



If L201 is not oscillator, changed L201 (220uH)

2) Check the RESET IC (U206-KIA7023AF)



If 3pin voltage is not 2.7V, changed RESET IC.

3) Check the LCD module line

Because of line short, D/G board not operated.

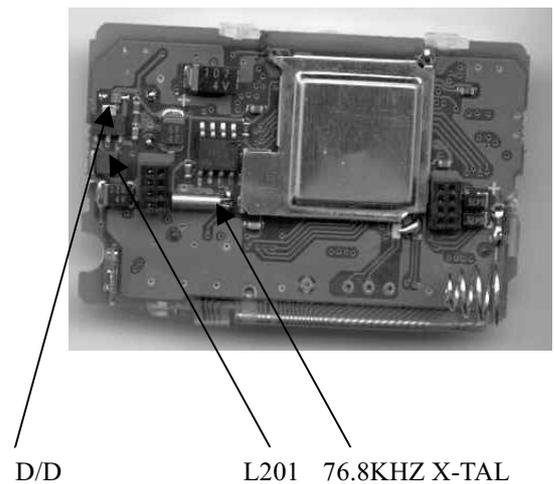
4) Check the S-RAM

If S-RAM defect, D/G board not operated.

5) Check the FONT IC

If FONT IC defect, D/G board not operated.

6) Check the 76.8KHZ x-tal



PROGRAM WRITING

Introduction

This section contains information for program writing with capcode and frequency etc.

CAUTION

This program uses only IBM comfortable PC.

Install

1. Program install

We provided diskette with capcode writing program as file name is "DPGMENG.EXE". So, Copy the all program in your PC.

2. Program fixture install

Connect RS-232C 9-pin connector of program fixture to COM1 or COM2 port of computer.

ACCESSORY COMPONENT

DC 5V ADAPTOR	1EA
PROGRAM FIXTURE	1EA
PROGRAM DISKETT	1EA

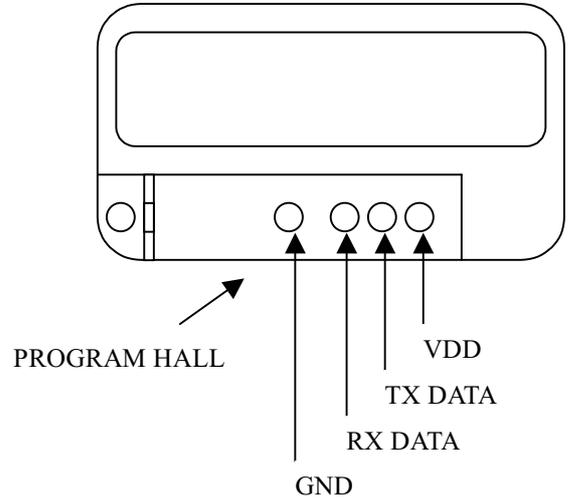
Program execute

File name: DPGMFREQ.EXE

Program methods

Set the programming with user option in writing program. Pick program hole of the front part with program fixture. And press "F5" key in computer keyboard for program. PC monitor is displayed data sending procedure. After program done, PC monitor is displayed "EEPROM write OK".

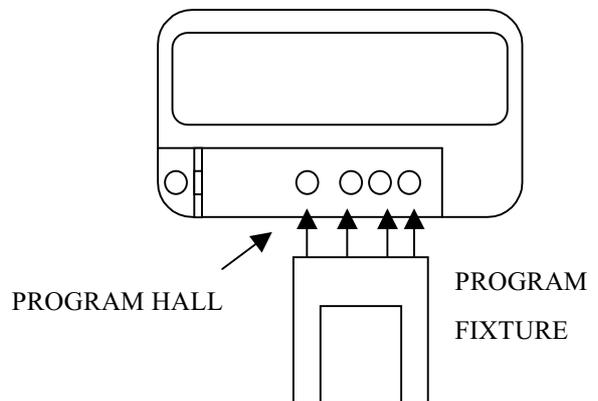
BACK PART



TROUBLE SHOOTING

Cannot program

1. Check about COM port setting status in program.
2. Check to COM port in PC.
3. Check the program fixture.
4. Check the pager status.
5. Check the pin 39, 40 in CPU with D/G board.
6. Check that DC ADAPTOR with fixture.



4.

Service Information

Introduction

This section contains information necessary to service the DAP-0X0.

Trouble shooting Equipment

Table 4-1 summarizes recommended equipment for troubleshooting the DAP-0X0.

Table 4-1

<u>Description</u>	<u>Application</u>
S.S.G	Signal sources.
Oscilloscope	View signal waveforms
Ant Fixture	Antenna fixture
Multimeter	Measure DC voltages
Frequency counter	Measure Frequency

Trouble shooting access

Set Equipment configures Figure 4-1 as follow;

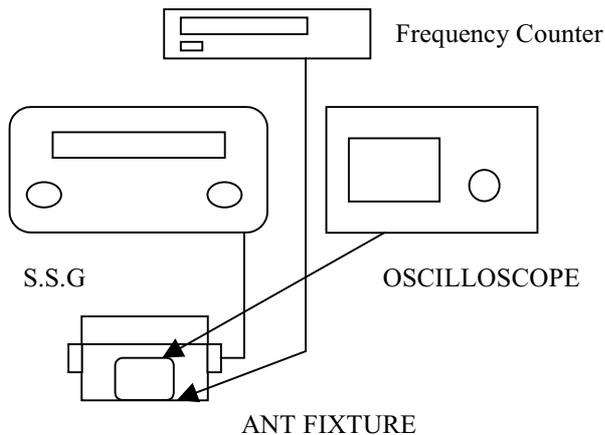


Figure 4-1 Equipment configure

Trouble shooting Procedure

Table 4-2 summarizes DAP-1X0 troubleshooting.

Table 4-2

Trouble shooting procedure.

Step	Component	<u>Comments</u>
1	LCD	No display No initial Broken segment
2	X201	No display
3	U205	No power
4	X202	No initial Out of key function
5	U206	No initial
6	U203	No initial
7	X111	Cannot receiver
8	VC112	Cannot receiver
9	L201	No power
10	U201	Broken Character No power
11	U202	Broken Character No power
12	CN202	Cannot receiver
13	CN201	Cannot receiver
14	LP201	No Back light
15	Q202	No back light

ASCII CODE for PAGER PROGRAM

Figure 4-2 ASCII CODE

SPACE	!	"	#	\$	%	&	'	()	*
00/20	21	22	23	24	25	26	27	28	29	2A
+	,	-	.	/	0	1	2	3	4	5
2B	2C	2D	2E	2F	30	31	32	33	34	35
6	7	8	9	:	;	<	=	>	?	@
36	37	38	39	3A	3B	3C	3D	3E	3F	40
A	B	C	D	E	F	G	H	I	J	K
41	42	43	44	45	46	47	48	49	4A	4B
L	M	N	O	P	Q	R	S	T	U	V
4C	4D	4E	4F	50	51	52	53	54	55	56
W	X	Y	Z	[\]	^	_	`	a
57	58	59	5A	5B	5C	5D	5E	5F	60	61
b	c	d	e	f	g	h	i	j	k	l
62	63	64	65	66	67	68	69	6A	6B	6C
m	n	o	p	q	r	s	t	u	v	w
6D	6E	6F	70	71	72	73	74	75	76	77
x	y	z	{		}	~				
78	79	7A	7B	7C	7D	7E				

DISPLAY DIMENSION

2 X 16
